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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/913,688	11/14/2001	Takeo Morinaga	SONYJP-135 3830	
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KRUMHOLZ & MENTLIK			NGUYEN, TANH Q	
600 SOUTH AVENUE WEST WESTFIELD, NJ 07090			ART UNIT	PAPER NUMBER
			2182	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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	Application No.	Applicant(s)				
0577 4 44 0	09/913,688	MORINAGA, TAKEO				
Office Action Summary	Examiner	Art Unit				
	Tanh Q. Nguyen	2182				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 6(a). In no event, however, may a reply be tim ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONEI	l. ely filed the mailing date of this communication. O (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on 22 Ju	Responsive to communication(s) filed on <u>22 June 2007</u> .					
·= ·	action is non-final.	n-final.				
,—	<u> </u>					
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1,2,7-20,25-38,41,43,45,46,48,49 and 51</u> is/are pending in the application.						
4a) Of the above claim(s) <u>8-18,25-34,36 and 38</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,2,7,19-20,35,37,41,43,45,46,48,49 and 51</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
,— ,,— ,	4					
Application Papers						
9) The specification is objected to by the Examiner.						
10) \square The drawing(s) filed on <u>27 June 2006</u> is/are: a) \square accepted or b) \square objected to by the Examiner.						
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the correct						
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 						
3. Copies of the certified copies of the prior		ed in this National Stage				
application from the International Bureau	• • • • • • • • • • • • • • • • • • • •	.d				
* See the attached detailed Office action for a list of the certified copies not received.						
	•					
Attachment(s)						
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date						

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DETAILED ACTION

Claim Objections

1. Claims 1, 41; 19, 43; 35, 46; 37, 49 are objected to because of the following informalities:

"index" in line 17 of claim 1 should be replaced with "an index".

"for mediating said packets **outputting** from said memory means" in lines 22-23 of claim 1 should be replaced with "for mediating said packets **outputted** from said memory means".

"said address of memory means" in line 35 of claim 1 should be replaced with said address of said memory means to avoid interpretation a second memory means.

"predetermined data amount" in line 36 of claim 1 should be replaced with "a predetermined data amount".

"said input FIFO for sequentially storing said packets for recording and for outputting said packets in storing order" in lines 3-4 of claim 41 should be replaced with "wherein said input FIFO sequentially stores said packets for recording and outputs said packets in storing order" - for clarity.

Claims 19, 43; 35, 46; 37, 49 recite limitations that are similar to the limitations recited in claims 1, 41. Claims 19, 43; 35, 46; 37, 49 are objected to on the same bases as claims 1, 41.

2. Claims 2, 20, 45, 48 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.

Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s)

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in proper dependent form, or rewrite the claim(s) in independent form.

Claim 2 recites "said transferring of said packets is made cluster by cluster, said cluster being of a predetermined data amount" in lines 3-4. The limitation appears to have been covered by the limitation "transferring said packets of predetermined data amount" in lines 35-36 of claim 1.

Claims 19-20; 35, 45; 37, 48 recite limitations that are similar to the limitations recited in claims 1-2. Claims 20, 45, 48 are objected to on the same basis as claim 2.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 51 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "setting the maximum LBA of the memory area of the transport stream into the register, the LBA can be automatically returned to the start LBA of the memory capacity" on page 23, lines 23-27, does not reasonably provide enablement for "wherein in said register the maximum address of the memory in the recording means is set for automatically returning to the start address" in lines 3-5 of claim 51. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate

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in scope with these claims. There is no indication that the maximum LBA of the memory area of the transport stream is the maximum address of the memory in the recording means.

5. Claims 1, 2, 7, 41, 51; 19, 20, 43; 35, 45-46; 37, 48-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "said packets" in several instances in lines 9-13. It is not clear whether "said packets" refers to the packets constructing the stream, or to the packets extracted by the extracting means.

Claim 1 recites "said packets added said address" in line 19. It is not clear what applicant intends to claim with the limitation.

Claim 1 recites "said packets extracted by said extracting means storing said memory means" in lines 21-22. It is not clear what applicant intends to claim with the limitation. Specifically, it is not clear how the extracting means can store the memory means.

Claim 1 recites "counting up said address of memory means each time transferring said packets of predetermined data amount" in lines 35-36. It is not clear what applicant intends to claim with the limitation.

Claim 1 recites several means (receiving means, control means, extracting means, memory means, memory control means, index adding means, packets transferring control means, address adding means), and it appears that some of the

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means may not be supported by a plurality of structures (e.g. index adding means), the examiner requests that applicant map out each of the means with the elements in the specification to clarify the scope of the claim and further the prosecution.

Claims 19, 35, 37 recite limitations that are similar to the limitations recited in claim 1. Claims 19, 20, 43; 35, 45, 46; 37, 48-49 are rejected on the same bases as claims 1, 2, 41.

Claim 1 further recites "the recording means" in line 15. There is insufficient antecedent basis for the limitation in the claim.

Claim 51 recites "wherein in said register the maximum address of the memory in the recording means is set for automatically returning to the start address" in lines 3-5. It is not clear how the maximum address of the memory in the recording means can be set for automatically returning to the start address in the register - as the recording means has only one maximum of the memory. It appears that critical steps and/or elements are omitted in the drafting of claim 51. Clarification is required.

6. The rejections that follow are based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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Patentability shall not be negatived by the manner in which the invention was made.

- 8. Claims 1-2, 7, 19-20, 35, 37, 41, 43, 45-46, 48-49, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA: pages 1-9 and FIG. 1) in view of Mergard (US 5,881,248).
- 9. <u>As per claim 1</u>, AAPA teaches an information processing apparatus [a digital broadcast receiving apparatus FIG. 1] comprising:

receiving means [12, 13, FIG. 1] for receiving a stream constructed by packets of a predetermined format under control of a control means [CPU 1, FIG. 1];

extracting means [21, FIG. 1] for extracting packets from the packets constructing said stream received by said receiving means;

memory means [23, FIG. 1] for storing said packets for recording;

memory control means [28, 1 - FIG. 1] for controlling writing said packets into said memory means, for controlling reading said packets from said memory means [page 5, lines 19-23], for issuing a command to prepare transferring [the host CPU executes the issuance of a command to the hard disk, the setting of the transfer start timing - page 8, lines 24-27], and for supplying a start address of a recording means [the host CPU executes the setting of the LBA at every block transfer of recording means 15, FIG. 1 - page 8, lines 24-27];

index adding means [1, 24 - FIG. 1] for adding an address of a sector of a minimum unit of recording on the recording means [the setting of the LBA by the host CPU - page 8, lines 24-27; the address of the minimum unit is expressed by an LBA - page 8, lines 12-13] as an index to said packets read out by said memory control means

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[LBA being used for address designation to access location on recording means - page 8, lines 1-19], and for outputting said packets with the added address to said recording means [for outputting said packets using the LBA to the recording means];

an arbiter [28, FIG. 1] for mediating said packets extracted by said extracting means and stored in said memory means, and for mediating said packets outputted from said memory means to said index adding means in response to an instruction from said memory control means [page 5, lines 19-23]; and

packets transferring control means [DMA controller - 29, FIG. 1] for permitting write access of said packets outputted from said index adding means to said recording means in accordance with said command from said memory control means [page 8, lines 14-16; page 8, lines 24-26], wherein said packets transferring control means includes an address determining means for starting an address of said recording means when said start address is inputted from said memory control means by counting up said address of memory means each time a cluster of a predetermined amount is transferred [a DMA controller implicitly includes a counter for tracking amount of data transferred as a DMA descriptor/command includes a length of the block transfer].

AAPA does not teach issuing the command before an amount of the packets stored by the memory means reaches a full capacity.

Mergard teaches forming a command when the data amount of the packets stored in the memory means reaches a predetermined capacity in order to prevent the memory from overflowing, the predetermined capacity being less than the full capacity of the memory [col. 7, lines 13-19].

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a DMA command when the data amount of the packets stored in the memory means reaches a predetermined capacity, as is taught by Mergard, in order to prevent the memory from overflowing.

- 10. As per claim 2, AAPA teaches the memory means including an input FIFO [23, FIG. 1], and the minimum unit of the recording of the data being a sector of a predetermined data amount [page 8, lines 1-3] hence said transferring of said packets being made cluster by cluster, the cluster being of a predetermined data amount.
- 11. As per claims 7, 19-20, AAPA further teach the recording means being a hard disk drive [15, FIG. 1] built in said information processing apparatus [FIG. 1].
- 12. As per claims 35, 37, the claims generally correspond to claim 1 and are rejected on the same bases.

As per claims 41, 43, AAPA teaches said input FIFO sequentially storing said packets for recording and outputting said packets in storing order [page 5, lines 15-17]; said packets transferring control means supplying a start address for the packets to be transferred.

- 13. As per claims 45-46, 48-49, see the rejections of claims 2 and 41 above.
- 14. <u>As per claim 51</u>, AAPA teaches said packets transferring control means further including a register for comparison of address of memory [a DMA controller inherently includes a register for comparison of address of memory to determine whether transfer is complete].

Response to Arguments

15. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hirahata et al. (JP 07-114510) discloses eliminating the need for DMA actuation by a processor and efficiently use a FIFO in an I/O - by providing a circuit which detects the conditions of DMA actuation and allowing an I/O to actuate DMA.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later

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than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TANH Q NGUYEN PRIMARY EXAMINER TECHNOLOGY CENTER 2100

TQN August 30, 2007